

AMENDMENTS TO THE CLAIMS

1 1. (Original) A method for forming a buried cavity in a semiconductor substrate formed
2 by at least a first wafer and a second wafer both of semiconductor material directly bonded along a
3 bond interface, the method comprising the steps of:

4 treating one of the first and second wafers to be selectively etchable adjacent a surface
5 thereof to form a selectively etchable portion prior to bonding of the first and second wafers,

6 bonding the first and second wafers together with the surface of the one of the first and
7 second wafers adjacent which the portion of the wafer is selectively etchable forming with a
8 surface of the other of the first and second wafers the bond interface,

9 forming a communicating opening through the first wafer to the selectively etchable
10 portion, and

11 etching the selectively etchable portion to form the buried cavity beneath the first wafer.

1 2. (Original) A method as claimed in Claim 1 in which the one of the first and second
2 wafers which is treated to be selectively etchable is treated through the surface thereof which is to
3 form the bond interface.

1 3. (Original) A method as claimed in Claim 1 in which the one of the first and second
2 wafers which is treated to be selectively etchable is treated by doping.

1 4. (Original) A method as claimed in Claim 3 in which the one of the first and second
2 wafers which is treated to be selectively etchable is doped by ion implantation through the surface
3 which is to form the bond interface.

1 5. (Original) A method as claimed in Claim 3 in which the one of the first and second
2 wafers which is treated to be selectively etchable is doped by atom diffusion through the surface
3 which is to form the bond interface.

1 6. (Original) A method as claimed in Claim 3 in which the one of the first and second
2 wafers which is treated to be selectively etchable is of p type material, and the wafer is doped to
3 form the selectively etchable portion as a p+ region.

1 7. (Original) A method as claimed in Claim 6 in which the one of the first and second
2 wafers which is to be treated to be selectively etchable is doped by boron, or species thereof.

1 8. (Original) A method as claimed in Claim 3 in which the one of the first and second
2 wafers which is treated to be selectively etchable is of n type material, and the wafer is doped to
3 form the selectively etchable portion as a n+ region.

1 9. (Original) A method as claimed in Claim 8 in which the one of the first and second
2 wafers which is treated to be selectively etchable is doped by a dopant selected from one or more
3 of the following dopants:

4 phosphorous,
5 arsenic, and
6 antimony,
7 or species thereof.

1 10. (Original) A method as claimed in Claim 3 in which the one of the first and second
2 wafers which is treated to be selectively etchable is doped at a level greater than 10^{18} atoms per cc.

1 11. (Original) A method as claimed in Claim 1 in which the one of the first and second
2 wafers which is treated to be selectively etchable is treated so that the depth of the selectively
3 etchable portion corresponds to the desired depth of the buried cavity.

1 12. (Original) A method as claimed in Claim 1 in which the one of the first and second

2 wafers which is treated to be selectively etchable is treated so that the area of the selectively
3 etchable portion corresponds to the desired area of the buried cavity.

1 13. (Original) A method as claimed in Claim 1 in which the one of the first and second
2 wafers which is treated to be selectively etchable is treated so that the area of the selectively
3 etchable portion extends substantially over the entire bond interface.

1 14. (Original) A method as claimed in Claim 1 in which the second wafer is treated to be
2 selectively etchable in its entirety, and a third wafer of semiconductor material is bonded to the
3 second wafer so that the second wafer is sandwiched between the third wafer and the first wafer.

1 15. (Original) A method as claimed in Claim 14 in which the third wafer is directly
2 bonded to the first wafer.

1 16. (Original) A method as claimed in Claim 1 in which the second wafer is treated to be
2 selectively etchable.

1 17. (Original) A method as claimed in Claim 1 in which the first wafer is treated to be
2 selectively etchable.

1 18. (Original) A method as claimed in Claim 1 in which the first and the second wafer
2 are treated to be selectively etchable, and the first and second wafers are bonded together with
3 their respective surfaces which are adjacent the portions thereof which are selectively etchable
4 forming the bond interface.

1 19. (Original) A method as claimed in Claim 1 in which the selectively etchable portion is
2 etched by a wet etch to form the buried cavity.

1 20. (Original) A method as claimed in Claim 1 in which the communicating opening is

2 formed in the first wafer by etching.

1 21. (Original) A method as claimed in Claim 20 in which the communicating opening is
2 etched in the first wafer by a reactive ion etch (RIE).

1 22. (Original) A method as claimed in Claim 1 in which an etch stop is formed in the
2 selectively etchable portion for defining the area of the buried cavity prior to etching of the
3 selectively etchable portion for limiting the etch in a lateral direction to form the buried cavity.

1 23. (Original) A method as claimed in Claim 22 in which the etch stop is formed in the
2 selectively etchable portion after bonding of the wafers.

1 24. (Original) A method as claimed in Claim 23 in which an etch stop forming trench is
2 formed through one of the wafers into the selectively etchable portion, and an etch stop material is
3 located in at least the portion of the etch stop forming trench in the selectively etchable portion for
4 forming the etch stop.

1 25. (Original) A method as claimed in Claim 24 in which the etch stop forming trench is
2 formed by etching.

1 26. (Original) A method as claimed in Claim 24 in which the etch stop forming trench is
2 etched by an RIE etch.

1 27. (Original) A method as claimed in Claim 24 in which the etch stop forming trench is
2 formed in the first wafer.

1 28. (Original) A method as claimed in Claim 1 in which the communicating opening is
2 formed in the first wafer adjacent the centre of the area of the first wafer which is to be above the

3 buried cavity, and the buried cavity is formed radiating laterally outwardly from and around the
4 communicating opening.

1 29. (Original) A method as claimed in Claim 1 in which a pair of communicating
2 openings are formed in the first wafer spaced apart from each other.

1 30. (Original) A method as claimed in Claim 1 in which the buried cavity is at least
2 partially filled with an electrically insulating material for forming a buried insulating layer beneath
3 the first wafer for forming with a portion of the first wafer above the buried insulating layer a
4 semiconductor-on-insulator (SOI).

1 31. (Original) A method as claimed in Claim 30 in which the electrically insulating
2 material with which the buried cavity is at least partially filled is an oxide.

1 32. (Original) A method as claimed in Claim 30 in which the electrically insulating
2 material with which the buried cavity is at least partially filled is deposited in the buried cavity.

1 33. (Original) A method as claimed in Claim 30 in which the electrically insulating
2 material with which the buried cavity is at least partially filled is grown in the buried cavity.

1 34. (Original) A method as claimed in Claim 1 in which an electrical isolation trench is
2 formed in the first wafer for electrically isolating an area of the first wafer above the buried
3 cavity.

1 35. (Original) A method as claimed in Claim 34 in which the electrical isolation trench is
2 at least partly filled with an electrically insulating material.

1 36. (Original) A method as claimed in Claim 34 in which the communicating opening is

2 located to form a part of the electrical isolation trench.

1 37. (Original) A method as claimed in Claim 36 in which the portion of the electrical
2 isolation trench which is not formed by the communicating opening, is formed after filling of the
3 buried cavity with the electrically insulating material.

1 38. (Original) A method as claimed in Claim 1 in which each communicating opening is
2 at least partially filled with an electrically insulating material.

1 39. (Original) A method as claimed in Claim 1 in which each communicating opening is
2 filled with an electrically insulating material.

1 40. (Original) A method as claimed in Claim 1 in which each communicating opening is
2 at least partially filled with polysilicon.

1 41. (Original) A method as claimed in Claim 1 in which each communicating opening is
2 filled with polysilicon.

1 42. (Original) A method as claimed in Claim 1 in which a plurality of discrete buried
2 cavities are formed in the semiconductor substrate.

1 43. (Original) A method as claimed in Claim 42 in which at least some of the buried
2 cavities are at least partially filled with the electrical insulating material for forming a plurality of
3 discrete SOIs.

1 44. (Original) A method as claimed in Claim 1 in which the first wafer is thinned after
2 the buried cavity has been formed.

1 45. (Original) A method as claimed in Claim 1 in which each wafer is of single crystal

2 silicon material.

1 46. (Original) A semiconductor substrate having a buried cavity therein, the
2 semiconductor substrate being formed by the method as claimed in Claim 1.

1 47. (Original) A semiconductor substrate having an SOI formed therein, the SOI being
2 formed by the method as claimed in Claim 30.

1 48. (Withdrawn) A semiconductor substrate having a buried cavity therein, the
2 semiconductor substrate comprising:

3 a first wafer of semiconductor material,

4 a second wafer of semiconductor material directly bonded to the first wafer along a bond
5 interface,

6 one of the first and second wafers having been treated to form a selectively etchable
7 portion adjacent a surface thereof prior to bonding of the first and second wafers, and

8 the buried cavity having been etched in the selectively etchable portion beneath the first
9 wafer through a communicating opening formed in the first wafer.

1 49. (Withdrawn) A semiconductor substrate having an SOI formed therein, the substrate
2 comprising:

3 a first wafer of semiconductor material,

4 a second wafer of semiconductor material directly bonded to the first wafer along a bond
5 interface,

6 one of the first and second wafers having been treated to form a selectively etchable
7 portion adjacent a surface thereof prior to bonding of the first and second wafers,

8 a buried cavity having been etched in the selectively etchable portion beneath the first

9 wafer through a communicating opening formed in the first wafer, and
10 an electrically insulating layer formed in the buried cavity for forming with a portion of the
11 first wafer above the buried insulating layer the SOI.